Release 14.7 - xst P.20131013 (lin64)

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Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.01 secs

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Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.01 secs

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Reading design: test.prj

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\* Synthesis Options Summary \*

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---- Source Parameters

Input File Name : "test.prj"

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "test"

Output Format : NGC

Target Device : xc7a100t-3-csg324

---- Source Options

Top Module Name : test

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 32

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As\_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

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\* HDL Parsing \*

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Analyzing Verilog file "/home/ise/circuit/test.vf" into library work

Parsing module <test>.

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\* HDL Elaboration \*

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Elaborating module <test>.

Elaborating module <OR2>.

Elaborating module <FD(INIT=1'b0)>.

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\* HDL Synthesis \*

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Synthesizing Unit <test>.

Related source file is "/home/ise/circuit/test.vf".

Summary:

no macro.

Unit <test> synthesized.

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HDL Synthesis Report

Found no macro

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\* Advanced HDL Synthesis \*

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Advanced HDL Synthesis Report

Macro Statistics

# Registers : 1

Flip-Flops : 1

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\* Low Level Synthesis \*

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Optimizing unit <test> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block test, actual ratio is 0.

Final Macro Processing ...

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Final Register Report

Macro Statistics

# Registers : 1

Flip-Flops : 1

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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\* Design Summary \*

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Top Level Output File Name : test.ngc

Primitive and Black Box Usage:

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# BELS : 3

# OR2 : 3

# FlipFlops/Latches : 1

# FD : 1

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 5

# IBUF : 4

# OBUF : 1

Device utilization summary:

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Selected Device : 7a100tcsg324-3

Slice Logic Utilization:

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 0

Number with an unused Flip Flop: 0 out of 0

Number with an unused LUT: 0 out of 0

Number of fully used LUT-FF pairs: 0 out of 0

Number of unique control sets: 1

IO Utilization:

Number of IOs: 6

Number of bonded IOBs: 6 out of 210 2%

IOB Flip Flops/Latches: 1

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 32 3%

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Partition Resource Summary:

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No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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Clock Signal | Clock buffer(FF name) | Load |

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Clk | BUFGP | 1 |

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Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: 2.659ns

Maximum output required time after clock: 0.640ns

Maximum combinational path delay: No path found

Timing Details:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default OFFSET IN BEFORE for Clock 'Clk'

Total number of paths / destination ports: 4 / 1

-------------------------------------------------------------------------

Offset: 2.659ns (Levels of Logic = 4)

Source: B (PAD)

Destination: XLXI\_4 (FF)

Destination Clock: Clk rising

Data Path: B to XLXI\_4

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 1 0.001 0.693 B\_IBUF (B\_IBUF)

OR2:I0->O 1 0.097 0.683 XLXI\_1 (XLXN\_2)

OR2:I1->O 1 0.107 0.683 XLXI\_2 (XLXN\_1)

OR2:I1->O 1 0.107 0.279 XLXI\_3 (D\_int)

FD:D 0.008 XLXI\_4

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Total 2.659ns (0.320ns logic, 2.339ns route)

(12.0% logic, 88.0% route)

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Timing constraint: Default OFFSET OUT AFTER for Clock 'Clk'

Total number of paths / destination ports: 1 / 1

-------------------------------------------------------------------------

Offset: 0.640ns (Levels of Logic = 1)

Source: XLXI\_4 (FF)

Destination: Q (PAD)

Source Clock: Clk rising

Data Path: XLXI\_4 to Q

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FD:C->Q 1 0.361 0.279 XLXI\_4 (Q\_OBUF)

OBUF:I->O 0.000 Q\_OBUF (Q)

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Total 0.640ns (0.361ns logic, 0.279ns route)

(56.4% logic, 43.6% route)

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Cross Clock Domains Report:

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Total REAL time to Xst completion: 4.00 secs

Total CPU time to Xst completion: 1.33 secs

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Total memory usage is 592628 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 (   0 filtered)